Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A method for writing a memory cell comprising:
providing a memory cell comprising an N-type well, three P-type doped regions formed on the N-type well, a first stacked dielectric layer formed on the N-type well and between a first doped region and a second doped region from among the three P-type doped regions, a first gate formed on the first stacked dielectric layer, a second stacked dielectric layer formed on the N-type well and between a second doped region and a third doped region from among the three P-type doped regions, a second gate formed on the second stacked dielectric layer;
applying a common voltage to the N-type well, the first doped region and the second gate;
applying a voltage less than the common voltage to the first gate in order to erase charges stored in the first stacked dielectric layer;
applying a first voltage to the first gate and a second voltage larger than the first voltage to the second gate, in order to conduct respectively P-type channels between the first doped region and the second doped region and the second doped region and the third doped region;

applying a voltage larger than the second voltage to the N-type well and the first doped region; and
applying a voltage less than the second voltage to the third doped region in order to inject channel hot hole induced hot electrons into the second stacked dielectric layer formed on the N-type well and between the second doped region and the third doped region.

[c2] 2.The method of claim 1wherein each stacked dielectric layer comprises:
a first silicon dioxide layer formed on the N-type well;
a charge storage layer formed on the first silicon dioxide layer; and
a second silicon dioxide layer formed on the charge storage layer.

[c3] 3.The method of claim 2wherein charge storage layer is composed of silicon nitride (Si_3N_4).

[c4] 4.The method of claim 2wherein charge storage layer is composed of silicon oxynitride ($Si_xN_yO_z$).

[c5] 5.A memory cell comprising:
an N-well;
three P-type doped regions formed on the N-type well;
a first stacked dielectric layer formed on the N-type well and between a first doped region and a second doped

region from among the three P-type doped regions;
a first gate formed on the first stacked dielectric layer;
a second stacked dielectric layer formed on the N-type well and between the second doped region and the third doped region from among the three P-type doped regions; and
a second gate formed on the second stacked dielectric layer.

[c6] 6.The memory cell of claim 5 wherein the first stacked dielectric layer can store charges and thereby change the threshold voltage for conducting a P-type channel between the first doped region and the second doped region.

[c7] 7.The memory cell of claim 5wherein each stacked dielectric layer comprises:
a first silicon dioxide layer formed on the N-type well;
a charge storage layer formed on the first silicon dioxide layer; and
a second silicon dioxide layer formed on the charge storage layer.

[c8] 8.The memory cell of claim 7wherein charge storage layer is composed of silicon nitride (Si_3N_4).

[c9] 9.The memory cell of claim 7wherein charge storage

layer is composed of silicon oxynitride ($Si_xN_yO_z$).

[c10] 10.A memory cell comprising:
a well with first doping type;
a first stacked dielectric layer formed on the said well and between two doped region with second doping type;
a first gate formed on the first stacked dielectric layer;
a second stacked dielectric layer formed on the said well and between two doped region with second doping type;
a second gate formed on the second stacked dielectric layer;
a said doped region of the said first stacked dielectric layer is electrically connected with a said doped region of the said second stacked dielectric layer.

[c11] 11.The memory cell of claim 10 wherein the first stacked dielectric layer can store charges and thereby change the threshold voltage for conducting the channel between the first doped region and the second doped region.

[c12] 12.The memory cell of claim 10 wherein each stacked dielectric layer comprises:
a first silicon dioxide layer formed on the well with first doping type;
a charge storage layer formed on the first silicon dioxide layer; and
a second silicon dioxide layer formed on the charge

storage layer.

[c13] 13.The memory cell of claim 12wherein charge storage layer is composed of silicon nitride (Si_3N_4).

[c14] 14.The memory cell of claim 12wherein charge storage layer is composed of silicon oxynitride ($Si_xN_yO_z$).